forming a first layer of silicon dioxide overlying a gate electrode of the flash memory cell;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer; and

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer after the oxidizing.

2. (Amended) The method of claim 1, wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min.

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3. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs at a pressure of approximately 1 atm. to 10 atm.

4. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

5. (Amended) The method of claim 2, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% steam to 100% steam.

6. (Amended) The method of claim 1, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s.

7. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs at a pressure of approximately 1 atm. to 10 atm.

8. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

9. (Amended) The method of claim 6, wherein oxidizing the silicon nitride layer occurs with a gas mixture of approximately 1% steam to 10% steam.

10. (Amended) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer; and

depositing a second layer of silicon dioxide on the silicon nitride layer after the oxidizing.

11. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

A1 End

12. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a batch furnace with a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% steam to 100% steam and a diluent, the diluent comprising one of argon and nitrogen.

13. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

14. (Amended) The method of claim 10, wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 1% steam to 10% steam and a diluent, the diluent comprising one of argon and nitrogen.

15. The method of claim 10, wherein the first layer of silicon dioxide is approximately 40Å to 70Å thick, the silicon nitride layer is approximately 50Å to 150Å thick, and the second layer of silicon dioxide is approximately 30Å to 50Å thick.

16. The method of claim 10, further comprising forming a second polysilicon layer on the second layer of silicon dioxide.

Please add new Claims 22-27 as follows:

22. (New) A method of forming a dielectric structure for a flash memory cell, the method comprising:

forming a first layer of silicon dioxide;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min.

23. (New) A method of forming a dielectric structure for a flash memory cell, the method comprising:

forming a first layer of silicon dioxide;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s.

24. (New) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min.

with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

25. (New) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a batch furnace with a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% steam to 100% steam and a diluent, the diluent comprising one of argon and nitrogen.

26. (New) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

27. (New) A method of making a flash memory cell including a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer on the first layer of silicon dioxide;

oxidizing the silicon nitride layer;

depositing a second layer of silicon dioxide on the silicon nitride layer after the oxidizing; and

wherein oxidizing the silicon nitride layer occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 1% steam to 10% steam and a diluent, the diluent comprising one of argon and nitrogen.